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(71) Applicant (for all designated States except US): **STMI-CROELECTRONICS S.R.L.** [IT/IT]; Via C. Olivetti, 2, I-20041 Agrate Brianza (IT).

(72) Inventors; and

(75) Inventors/Applicants (for US only): **PIDUTTI, Albino** [IT/IT]; Via Joppi, 42, I-33100 Udine (IT). **ADRAGNA, Claudio** [IT/IT]; Via Ardigò, 11, I-20052 Monza (IT). **FAGNANI, Mauro** [IT/IT]; Via per Villanova, 5, I-20014 Nerviano (IT).

(74) Agent: **MITTLER, Enrico**; Mittler & C. S.r.l., Viale Lombardia, 20, I-20131 Milano (IT).

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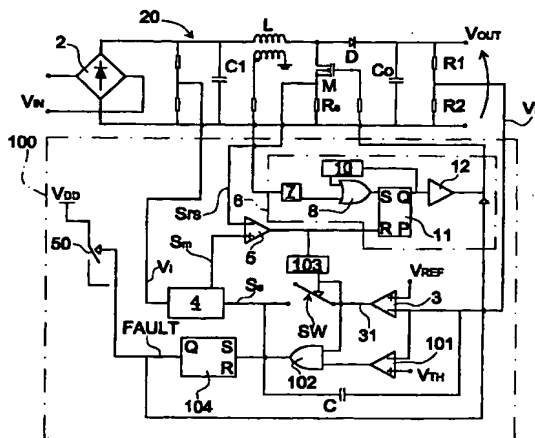
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(54) Title: **POWER FACTOR CORRECTION DEVICE FOR SWITCHING POWER SUPPLIES**



(57) Abstract: A power factor correction device for switching power supplies is described, which comprises a converter (20) and a control device (100;200;300) coupled with said converter (20) in such a way as to obtain from a input network alternated voltage (Vin) a direct regulated voltage (Vout) at the output terminal. The converter (20) comprises a power transistor (M) and the control device (100;200;300) comprises an error amplifier (3) having in input at the inverting terminal a first signal (Vr) proportional to said regulated voltage (Vout) at the non-inverting terminal a voltage reference (Vref), at least one capacitor (C) having a first terminal and a second terminal which are coupled respectively with the inverting terminal and the output terminal (31) of the error amplifier (3) and a driving circuit (4-6) of said power transistor (M) which is coupled with the second terminal of said capacitor (C). The control device (100;200;300) comprises interruption means (SW) placed between the output terminal (31) of said error amplifier (3) and said driving circuit (4-6) for at least one time period (T) lower than the time period (Ticlo) in which said control device (100; 200; 300) is operative.

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"Power factor correction device for switching power supplies."

\* \* \* \* \*

#### DESCRIPTION

5 The present invention relates to a power factor correction device for switching power supplies.

It is usually known to use devices to actively correct the power factor (PFC) for switching power supplies used in electronic equipments in common use as computers, televisions, monitors, etc. and for supplying fluorescent lamps, that is switching pre-regulator stages that must absorb  
10 from the external network a current that is almost sinusoidal and in phase with the network voltage. Therefore a switching power supply of the actual type comprises a PFC and a DC-DC converter connected with the output of the PFC.

A switching power supply of the traditional type comprises a DC-DC  
15 converter and an input stage connected with the electric network and constituted by a full wave rectifier diode bridge and by a capacitor connected immediately downstream for producing a not-regulated continuous voltage that derives from the alternated sinusoidal network voltage. The capacitor has a capacity great enough that a relative low undulation with respect to the  
20 continuos level is present at its terminals. The rectifier diodes of the bridge also will conduct only for a small portion of each half cycle of the network voltage because the instantaneous value thereof is lower than the voltage at the terminals of the capacitor for the greatest part of the cycle. Consequently the current adsorbed from the network will be constituted by a series of  
25 narrow pulses the amplitude of which is 5-10 times the resulting average value.

This presents considerable consequences: the current adsorbed from the network has peak values and efficacious values which are much higher than those in the case of adsorbing sinusoidal current, the network voltage is  
30 distorted due to the almost simultaneous pulse adsorption of all the users

connected with the network, in the case of three-phase systems the current in the neutral conductor is increased and a low use of the power potentialities of the electric power systems occurs. In fact, the pulse current waveform has many odd harmonics which, even if do not contribute to the power supplied to the load, contribute to increase the efficacious current adsorbed from the network and also to increase the power dissipation.

Quantitatively this can be expressed both as Power Factor (PF), that is the ratio between the real power (that supplied to the load by the power supply which is added to the power dissipated internally as heat), and the apparent power (the product of the network efficacious power by the absorbed efficacious power), and as Total Harmonic Distortion (THD), which usually is the percent ratio between the energy associated to all the superior level harmonics and that associated to the main harmonic. Usually a power supply provided with a capacitive filter has a PF comprised between 0.4 and 0.6 and a THD higher than 100%.

A PFC, placed between the rectifier bridge and the input of the DC-DC converter, allows to adsorb from the network a current which is almost sinusoidal and in phase with the voltage, by making the PF near 1 and by reducing the THD.

In Figure 1 a pre-regulator PFC stage is schematically shown comprising a boost converter 20 and a control device 1, in this case the control device L6561 produced by STMicroelectronics S.p.A.. The boost converter 20 comprises a full wave diode rectifier bridge 2 having in input a network voltage  $V_{in}$ , a capacitor C1 (which serves as filter for the high frequency) having one terminal connected with the diode bridge 2 and the other terminal connected to ground, an inductor L connected with a terminal of the capacitor C1, a MOS power transistor M having the drain terminal connected with a terminal of the inductor L downstream of the last one and which has the source terminal connected with a resistor  $R_s$  connected to ground, a diode D having the anode connected with the common terminal of

the inductor L and of the transistor M and the cathode connected with a capacitor Co having the other terminal connected to ground. The boost converter 20 generates an output direct voltage Vout at the terminals of the capacitor Co which is higher than the highest peak of the network voltage, typically 400V for systems supplied by a European network or by means of a universal supply. Such voltage Vout will be the input voltage of the DC-DC converter connected with the PFC.

The control device 1 must keep the output voltage Vout at a constant value by means of a feedback control action. The control device 1 comprises an error operational amplifier 3 adapted to compare a part of the output voltage Vout, which is the voltage Vr given by  $V_r = R_2 \cdot V_{out} / (R_2 + R_1)$  (wherein the resistors R1 and R2 are connected in series with each other and are connected in parallel with the capacitor Co) with a voltage reference Vref, for example of the value of 2.5V, and it generates an error signal proportional to the difference thereof. The output voltage Vout presents an undulation at a frequency that is twice the network frequency and which is superimposed to the continuous value. However if the bandwidth of the error amplifier is considerably reduced (typically it is lower than 20 Hz) by means of a suitable compensation network comprising at least one capacitor and if an operation in almost stationary regime is assumed, that is if the input efficacious voltage and the load are constant, such undulation will be considerably reduced and the error signal will become constant.

The error signal Se is sent to a multiplier 4 wherein it is multiplied by a signal Vi that is a part of the network voltage rectified by the diode bridge 2. At the output of the multiplier 4 a signal Sm will occur which is given by a rectified sinusoid the width thereof will depend certainly on the network efficacious voltage and on the error signal Se.

The signal Sm is sent to the non-inverting input of a PWM comparator 5 while at the inverting input the signal Srs is applied which occurs on the resistance Rs. If the signals Srs and Sm are equal the comparator 5 sends a

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signal to the control block 6 adapted to drive the transistor M and which, in this case, provides to turn off it. In such way the output signal  $S_m$  of the multiplier determines the peak current of the transistor M and it will be enveloped by a rectified sinusoid. A filter placed at the input of the stage eliminates the component at the commutation frequency and provides the current adsorbed from the network to have the shape of the sinusoidal envelope. The block 6 comprises a block 7 adapted to detect the current zeros and able to send a pulse signal to an OR gate 8 the other input terminal of which is connected with a starter 10, adapted to send a signal to the OR gate 8 at start time instant; the output signal S of the OR gate 8 is the set input of the set-reset flip-flop 11 having another input R that is the output signal of the device 5, and which has an output signal Q. The signal Q is sent at the input of a driver 12 which controls the turning on and off of the transistor M.

The error amplifier 3 may be formed in two different ways: as a voltage amplifier, wherein the output voltage is proportional to the difference between the voltages at the input terminals, or as a transconductance amplifier, the output current of which is proportional to the difference between the voltages that are present at the input terminals. The use of the voltage amplifier as error amplifier is preferable for higher noise immunity thereof as in the aforementioned device L6561.

Since it is necessary to modify the transfer function of the loop gain for all the closed loop feedback control systems in order to assure the stability of the same loop and to provide for a satisfactory dynamic operation, in the case of the PFCs this is performed usually by modifying the frequency response of the error amplifier. By using a voltage amplifier as error amplifier, the compensation network comprises at least one capacitor C connected in feedback between the output and the inverting input of the amplifier 3.

One among the possible faults for a switching power supply provided

with a PFC is the opening of the voltage control loop.

The more usual cause is due to the breaking of the resistor R1 of the output divider which is connected to the high voltage: in such case the system loses the information of the output voltage and the resistor R2 is inclined to bring the input of the error amplifier to ground. In such way the output is unbalanced towards the top and therefore the turning on of the transistor M is controlled for the maximum possible duration. Consequently the output voltage will increase without control bringing the load supplied by the PFC and the same PFC to destruction.

By using the error amplifier 3, the presence of the compensation network with the capacitor C connected between the output and the inverting input determines that the latter has the same potential of the other input for the whole period wherein the current may flow through the capacitor C, that is until the output of the error amplifier 3 has the possibility of increasing. When the output arrives at the top end of its dynamic or, as it is called, the error amplifier 3 is saturated high, the current does not flow through the capacitor and the inverting input may go to ground.

In commerce there are integrated PFCs having a protection against the opening of the voltage control loop. The solution in such PFCs consists of adding a further resistive divider (constituted by the resistors R1a and R2a which are connected in series with each other) connected with the output of the PFC which allows to read the voltage and to use a further comparator 28 having the non-inverting input connected with a reference voltage Vth1. When the resistor R1a is opened, the voltage at the inverting input of the comparator 28 overcomes the voltage Vth1 and the output 29 of the comparator 28 will provide to turn off the transistor M.

This solution has the disadvantage to require either external components (a comparator and a reference voltage generator with respective passive components besides the resistor divider) or, in the case of integrated formation, an added pin dedicated to this function which is in the control

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device 1 of the PFC. In the last case it is possible to incur to a lack of available pins, thereby resulting impossible to integrate this function.

In view of the state of the art described, it is an object of the present invention to provide a power factor correction device for switching power supplies which overcomes the aforementioned disadvantages.

According to present invention, such object is obtained by means of a power factor correction device for switching power supplies, comprising a converter and a control device coupled with said converter in such a way as to obtain from a input network alternated voltage a direct regulated voltage at the output terminal, said converter comprising a power transistor and said control device comprising an error amplifier having in input at the inverting terminal a first signal proportional to said regulated voltage and at the non-inverting terminal a voltage reference, at least one capacitor having a first terminal and a second terminal which are coupled respectively with the inverting terminal and the output terminal of said error amplifier and a driving circuit of said power transistor which is coupled with the second terminal of said capacitor, characterized in that said control device comprises interruption means placed between the output terminal of said error amplifier and the second terminal of said capacitor and control means able to activate said interruption means so as to control the interruption of the connection between the error amplifier and said driving circuit for at least one time period lower than the time period in which said control device is operative.

Preferably said control device comprises comparison means adapted to compare the value of said first signal with a reference value, said comparison means being able to send a signal adapted to deactivate said power transistor and said control device when the connection between said error amplifier and said drive circuit is interrupted and when the value of said first signal is lower than the value of said reference signal.

Thanks to present invention it is possible to form a power factor

correction device for switching power supplies which allows to protect the same PFC device when the value of the signal proportional to the output voltage and in input to the control device of the PFC goes to ground due to an opening of the control loop.

5           The features and the advantages of the present invention will be made evident by the following detailed description of embodiments thereof, shown as not limiting examples in the annexed drawings, wherein:

Figure 1 is a circuit scheme of a PFC for a switching power supply according to the prior art;

10           Figure 2 shows a prior art circuit solution for the protection of the PFC in Figure 1 in the case of the opening of the voltage loop;

Figure 3 is a circuit scheme of a PFC for a switching power supply according to a first embodiment of the present invention;

15           Figure 4 is a circuit scheme of a PFC for a switching power supply according to a variant of a first embodiment of the present invention;

Figure 5 is a circuit scheme of a PFC for a switching power supply according to a second embodiment of the present invention.

20           In Figure 3 a circuit scheme of a PFC for a switching power supply according to a first embodiment of the present invention is shown; the elements equal to the circuit of Figure 1 will be indicated by means of the same references. The PFC comprises a converter 20 provided with a full wave diode rectifier bridge 2 having in input a network voltage  $V_{in}$ , a capacitor C1 (which serves as filter for the high frequency) having one terminal connected with the diode bridge 2 and the other terminal connected to ground, an inductor L connected with a terminal of the capacitor C1, a MOS power transistor M having the drain terminal connected with a terminal of the inductor L downstream of the last and which has the source terminal connected with a resistor  $R_s$  connected to ground, a diode D having the anode connected with the common terminal of the inductor L and of the transistor M and the cathode connected with a capacitor  $C_o$  having the other

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terminal connected to ground. The boost converter 20 generates an output direct voltage  $V_{out}$  at the terminals of the capacitor  $C_o$  which is higher than the highest peak of the network voltage, typically 400V for systems supplied by a European network or by means of an universal supply. Such voltage  
5  $V_{out}$  will be the input voltage of the DC-DC converter connected with the PFC.

The PFC comprises a control circuit 100 able to keep the output voltage  $V_{out}$  at a constant value by means of a feedback control action. The control device 1 comprises an error amplifier 3 adapted to compare a part of  
10 the output voltage  $V_{out}$ , which is the voltage  $V_r$  given by  $V_r = R_2 * V_{out} / (R_2 + R_1)$  (wherein the resistors  $R_1$  and  $R_2$  are connected in series with each other and are connected in parallel with the capacitor  $C_o$ ) with a voltage reference  $V_{ref}$ , for example of the value of 2.5V, and it generates an error signal  $S_e$  proportional to the difference thereof. The  
15 output voltage  $V_{out}$  presents an undulation at a frequency that is twice the network frequency and which is superimposed to the direct value. However if the bandwidth of the error amplifier is considerable reduced (typically it is lower than 20 Hz) by means of a suitable compensation network comprising at least one capacitor and if an operation in almost stationary regime is  
20 assumed, that is if the input efficacious voltage and a load which are constant, such undulation will be considerable reduced and the error signal will become constant.

The error signal  $S_e$  is sent to a multiplier 4 wherein it is multiplied by a signal  $V_i$  that is a part of the network voltage rectified by the diode bridge  
25 2. At the output of the multiplier 4 a signal  $S_m$  will occur which is given by a rectified sinusoid the width thereof will depend certainly on the network efficacious voltage and on the error signal  $S_e$ .

The signal  $S_m$  is sent to the non inverting input of a PWM comparator  
5 while at the inverting input the signal  $S_{rs}$  is applied which occurs on the resistance  $R_s$ . If the signals  $S_{rs}$  and  $S_m$  are equal the comparator 5 sends a  
30

signal R to the set-reset flip-flop 11 belonging to the control block 6 for controlling the turning off of the transistor M

5 The block 6 comprises a block 7 adapted to detect the current zeros and able to send a pulse signal to the OR gate 8 the other input terminal of which is connected with a starter 10, adapted to send a signal to the OR gate 8 at the start time instant; the output signal S of the OR gate 8 is the set input of the set-reset flip-flop 11 having another input R that is the output signal of the device 5, and which has an output signal Q. The signal Q is sent to the input of a driver 12 which controls the turning on and off of the transistor M.

10 In such a way the output signal  $S_m$  of the multiplier determines the peak current of the transistor M and it will be enveloped by a rectified sinusoid. A filter placed at the input of the stage eliminates the component at the commutation frequency and provides the current adsorbed from the network to have the shape of the sinusoidal envelope.

15 The control circuit 100 comprises also a comparator 101 having the voltage signal  $V_r$  at the inverting input terminal and a voltage reference  $V_{th}$  at the non-inverting terminal. The output of the comparator is connected with one input of an AND gate 102 at the other input of which is present the output signal of a monostable multivibrator 103 controlled by the output  
20 signal of the PWM comparator 5. Alternatively the multivibrator 103 may be activated by a signal P, that is the denied signal Q, which is at the output of the flip-flop 11. The output of the AND gate 102 is connected with a set-reset flip-flop 104.

25 A switch SW is placed between the output terminal 31 of the error amplifier 3 and the terminal of the capacitor C which is coupled with the output of the error amplifier 3 and is controlled so as to interrupt the flow of the signal  $S_e$  into the analogic multiplier for a time period T when the comparator 5 sends the reset signal R to the flip-flop 11. The time period T is a small duration time period, for example  $1\mu s$ , that occurs in each  
30 operation cycle of the control device 100, that is for each period  $T_{ciclo}$

comprising the on time  $T_{on}$  of the MOS transistor M and the off time  $T_{off}$  of the same transistor M.

In such way, by having the input terminal of the multiplier 4 disconnected from the output terminal of the error amplifier 3, if the resistor R1 is opened, the voltage  $V_r$  at the inverting input terminal of the error amplifier 3 goes immediately to ground. The comparator 101 detects such operation condition and sends a signal to the AND gate 102 which activates the flip-flop 104 able to send an output signal Fault (that is the signal Q of the flip-flop 104) that allows to interrupt the supply of the control circuit 100 by acting on the switch 50 placed between a supply voltage VDD and the circuits belonging to the control device 100; this determines the turning off of the PFC.

In Figure 4 a circuit scheme of a PFC for a switching power supply according to a variant of the first embodiment of the present invention is shown. The PFC comprises the converter 20 and a control circuit 200 that is similar to the control circuit 100 in Figure 3 except for comprising a holding sampling device 201 that is placed between the switch SW and the analogic multiplier 4 and which is driven by the output terminal of the PWM comparator 5. The device 201 memorizes the value of the output signal  $Se$  of the error amplifier 3 when the reset signal R is emitted. In such way the disturbances that may be inducted in the multiplier 4 during its normal operation because of the opening of the switch SW are reduced.

In Figure 5 a circuit scheme of a PFC for a switching power supply according to a second embodiment of the present invention is shown. The PFC comprises a converter 20 and a control circuit 300 that is similar to the control circuit 100 in Figure 3 except for comprising a device 301 able to measure the current  $Se$  furnished by the error amplifier 3 and which is placed between the input of the multiplier 4 downstream of the switch SW and the compensation capacitor C. Said current  $Se$  is compared with a current reference inside the device 301 and, if the current  $Se$  is higher than

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the current reference, it sends to the output a signal S which, in combination with the reset signal R sent by the PWM comparator 5, determines the opening of the switch SW. More in detail the control circuit 300 comprises also a set-reset flip-flop 302 the set signal of which is the signal S of the  
5 device 301 and the reset signal is the output signal of the multivibrator 102; an AND gate 303 having in input the output signal Q of the flip-flop 302 and the denied output signal of the multivibrator 103 controls the switch SW which therefore is no longer controlled directly by the output signal of the multivibrator 103. The flip-flop 302 allows to avoid oscillations of the  
10 switch.

Therefore by means of the control circuit 300 the switch SW is opened for a time period T having a prefixed duration, determined by the monostable multivibrator 103 and for example  $1\mu\text{s}$ , only if the current  $I_{\text{se}}$  is higher than the current reference inside the device 301, where the time  
15 period T is lower than the time period  $T_{\text{ciclo}}$  that is the time period in which the control device 300 is operative.

In all the circuit structures that are present in Figures 3, 4 and 5, the indicated circuit components belonging to the control circuits 100, 200 and 300 are integrated in the same chip.  
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## CLAIMS

1. Power factor correction device for switching power supplies, comprising a converter (20) and a control device (100; 200; 300) coupled with said converter (20) in such a way as to obtain from a input network  
5 alternated voltage ( $V_{in}$ ) a direct regulated voltage ( $V_{out}$ ) at the output terminal, said converter (20) comprising a power transistor (M) and said control device (100; 200; 300) comprising an error amplifier (3) having in input at the inverting terminal a first signal ( $V_r$ ) proportional to said regulated voltage ( $V_{out}$ ) and at the non-inverting terminal a voltage  
10 reference ( $V_{ref}$ ), at least one capacitor (C) having a first terminal and a second terminal which are coupled respectively with the inverting terminal and the output terminal (31) of said error amplifier (3) and a driving circuit (4-6) of said power transistor (M) which is coupled with the second terminal of said capacitor (C), characterized in that said control device (100; 200;  
15 300) comprises interruption means (SW) placed between the output terminal (31) of said error amplifier (3) and the second terminal of said capacitor (C) and control means (103; 103, 301-303) able to activate said interruption means (SW) so as to control the interruption of the connection between the error amplifier (3) and said driving circuit (4-6) for at least one time period  
20 (T) lower than the time period ( $T_{iclo}$ ) in which said control device (100; 200; 300) is operative.

2. Device according to claim 1, characterized in that said control device (100; 200; 300) comprises comparison means (101) adapted to compare the value of said first signal ( $V_r$ ) with a reference value ( $V_{th}$ ), said comparison  
25 means (101) being able to send a signal (Fault) adapted to deactivate said power transistor (M) and said control device (100; 200; 300) when the connection between said error amplifier (3) and said drive circuit (4-6) is interrupted and when the value of said first signal ( $V_r$ ) is lower than the value of said reference signal ( $V_{th}$ ).

30 3. Device according to claim 1 or 2, characterized in that said at least

one time period (T) is constituted by a prefixed duration time period for each operation cycle (Tciclo) of the device (100; 200).

4. Device according to claim 3, characterized in that said converter (20) comprises a rectifier diode circuit (2) and said driving circuit (4-6) comprises a multiplier (4) coupled with said error amplifier (3) and which is adapted to multiply the output signal (Se) of said error amplifier (3) and of said capacitor (C) and a signal (Vi) proportional to the output signal of said rectifier diode circuit (2), a comparator (5) able to compare an output signal (Sm) of the multiplier (4) with a further signal (Srs) proportional to the current flowing in said power transistor (M), said control means (103) being connected with the output of said comparator (5) and being activated when the value of said output signal (Sm) of the multiplier (4) is equal to the value of said further signal (Srs) proportional to the current flowing in said power transistor (M).

5. Device according to claim 4, characterized in that said control means (103) are constituted by a monostable multivibrator that, when it is activated, is able to send a pulse signal to activate said interruption means (SW).

6. Device according to claim 5, characterized by comprising sampling means (201) connected with said multiplier (4), with the second terminal of the capacitor (C) and with the output of said comparator (5) and which are adapted to memorize the value of the output signal (Se) of the error amplifier (3) and of the capacitor (C) when said control means (103) are activated.

7. Device according to claim 1 or 2, characterized in that said at least one time period (T) is constituted by a prefixed duration time period and occurs when the value of the output signal (Se) of the error amplifier (3) and of the capacitor (C) is higher than a prefixed value.

8. Device according to claim 7, characterized in that said converter (20) comprises an input stage comprising a rectifier diode circuit (2) and said driving circuit (4-6) comprises a multiplier (4) coupled with said error amplifier (3) and which is adapted to multiply the output signal (Se) of said

error amplifier (3) and of said capacitor (C) and a signal ( $V_i$ ) proportional to the output signal of said rectifier diode circuit (2), a comparator (5) able to compare an output signal ( $S_m$ ) of the multiplier (4) with a further signal ( $S_{rs}$ ) proportional to the current flowing in said power transistor (M), said control means (103, 301-303) comprising a monostable multivibrator (103) connected with the output of said comparator (5) and which is activated when the value of said output signal ( $S_m$ ) of the multiplier (4) is equal to the value of said further signal ( $S_{rs}$ ) proportional to the current flowing in said power transistor (M) and detecting means (301) able to detect the value of the current flowing through said capacitor (C) and to compare said value with a current reference so as to send an output signal when said current is higher than said current reference, said output signal of said detecting means being able to activate said interruption means (SW) when said monostable multivibrator (103) is activated.

9. Device according to claim 6 or 8, characterized in that said control device (100; 200; 300) comprises comparison means (101) adapted to compare the value of said first signal ( $V_r$ ) with a reference signal ( $V_{th}$ ), said comparison means (101) being able to send a signal (Fault) adapted to deactivate said power transistor (M) and said control device (100; 200; 300) when the connection between said error amplifier (3) and said driving circuit (4-6) is interrupted and when the value of said first signal ( $V_r$ ) is lower than the value of said reference signal ( $V_{th}$ ), an AND gate (102) having in input the output signal of said monostable multivibrator (103) and the output signal of said comparison means (101), the output signal of said AND gate (102) being the set signal of a set-reset flip-flop (104) the output signal of which is said signal (Fault) adapted to deactivate said power transistor (M) and said control device (100; 200; 300).

10. Device according to claim 9, characterized in that said control means (103; 301-303), said interruption means (SW) and said comparison means (101) are integrated in the same chip where the control device (100; 200;

- 15 -

300) is formed.

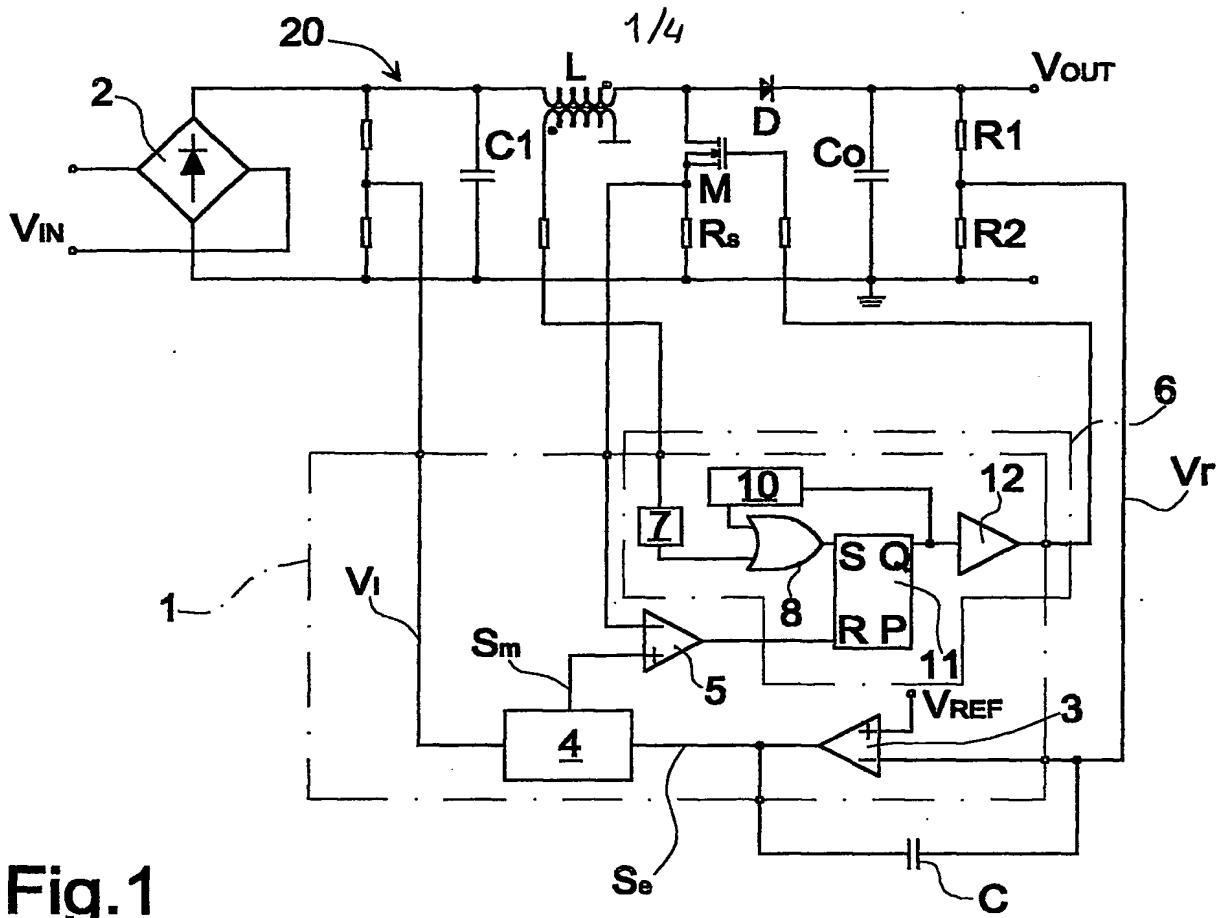


Fig.1

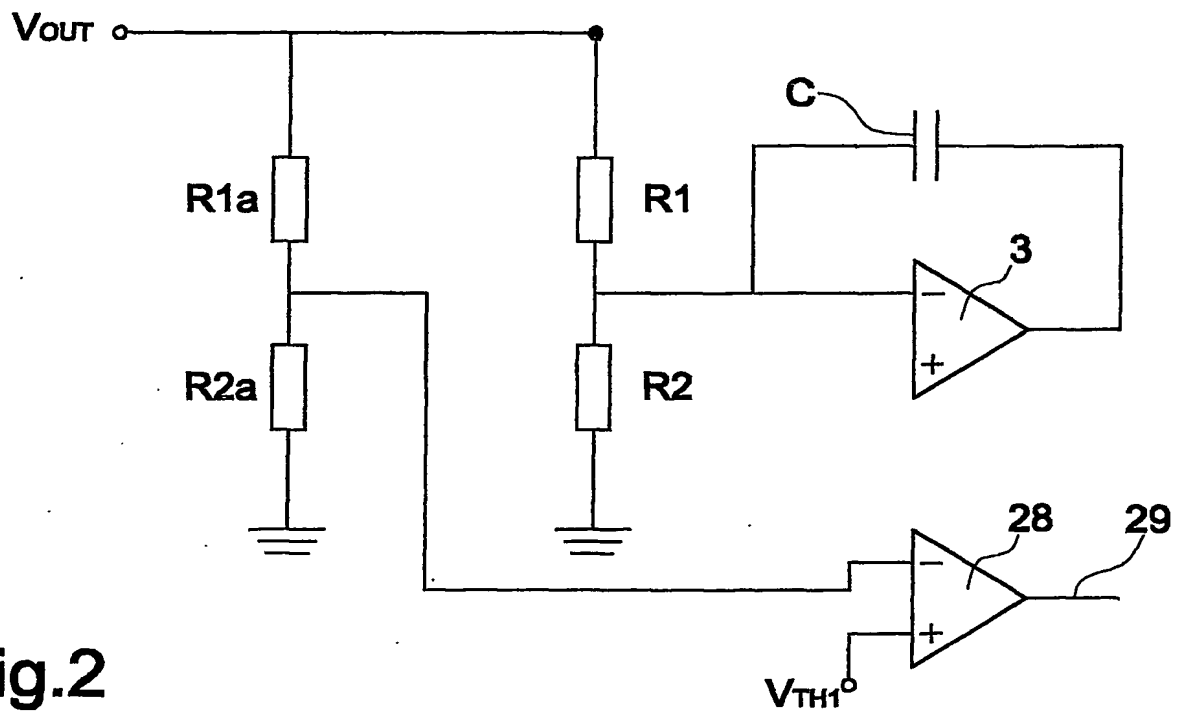
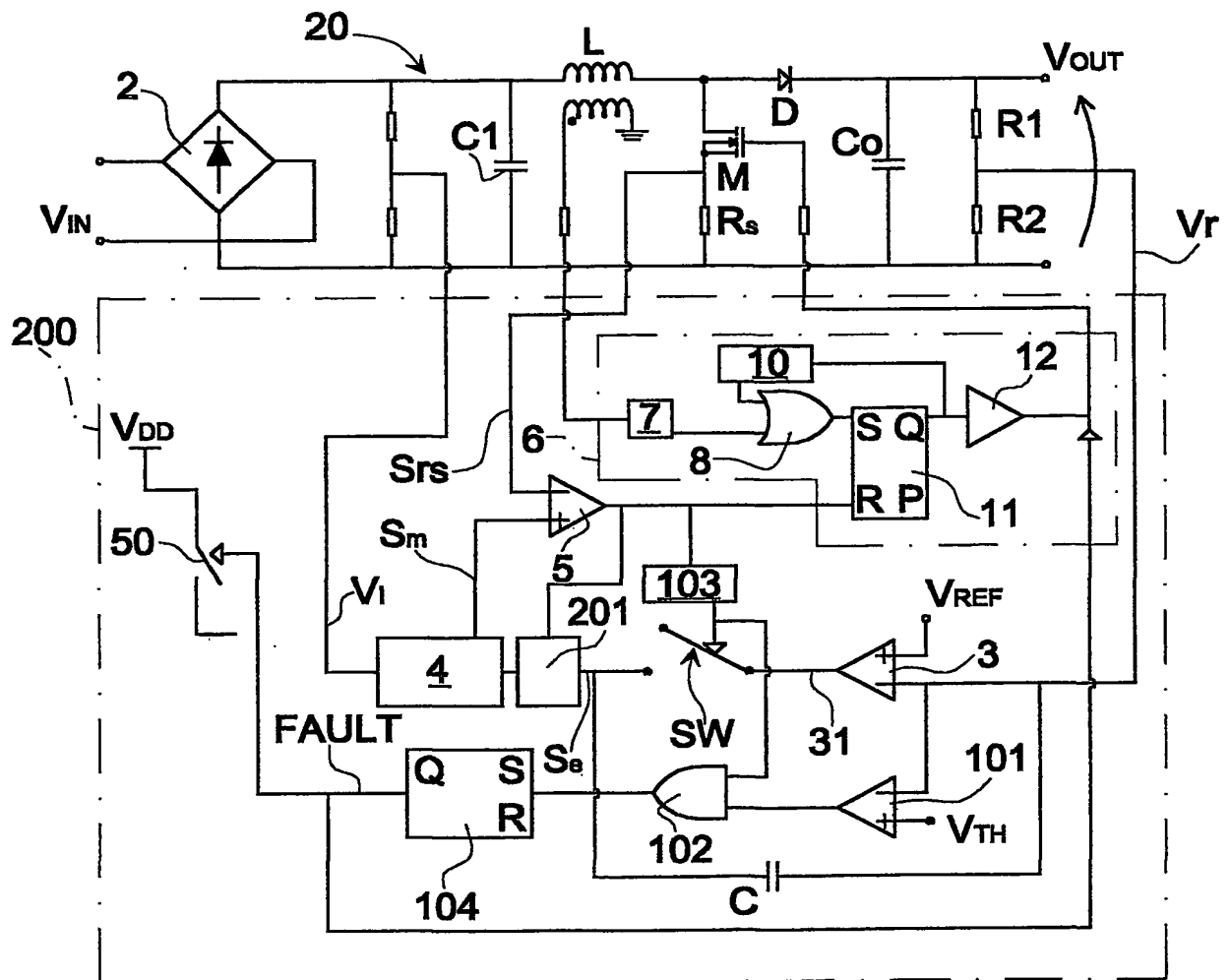
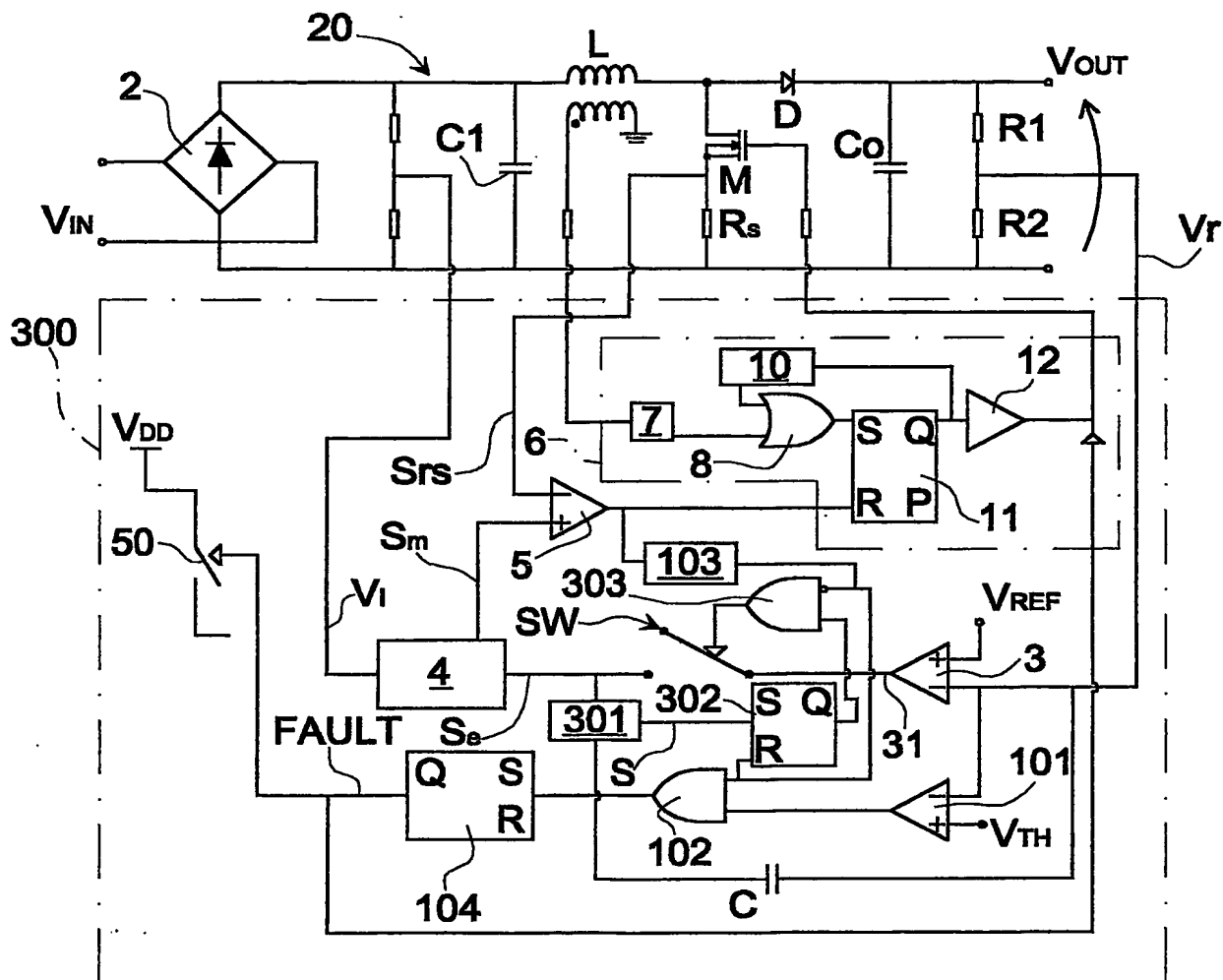


Fig.2



$\frac{3}{4}$ 

4/4



**Fig.5**

# INTERNATIONAL SEARCH REPORT

International Application No  
PCT/IT02/00602

A. CLASSIFICATION OF SUBJECT MATTER  
IPC 7 H02M1/00

According to International Patent Classification (IPC) or to both national classification and IPC

## B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)  
IPC 7 H02M

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal

## C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	ST L6561 Power Factor Corrector Februaury 2001 page 1/11-11/11 XP002245083 cited in the application the whole document	1-10
A	WO 02 52708 A ( EMERSON NETWORK POWER CO LTD ) 4 July 2002 (2002-07-04) figures 1,2,3,4A,4B	1-10
A	DE 100 42 587 A (INFINEON TECHNOLOGIES AG) 14 March 2002 (2002-03-14) abstract column 2; figure 1	1-10

☐ Further documents are listed in the continuation of box C.

☒ Patent family members are listed in annex.

### \* Special categories of cited documents :

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Date of the actual completion of the international search

23 June 2003

Date of mailing of the international search report

02/07/2003

Name and mailing address of the ISA  
European Patent Office, P.B. 5818 Patentlaan 2  
NL - 2280 HV Rijswijk  
Tel. (+31-70) 340-2040, Tx. 31 651 epo nl,  
Fax: (+31-70) 340-3016

Authorized officer

Marannino, E.

# INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No

PCT/IT<sup>99</sup>/02/00602

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
WO 0252708 8	A	NONE	
DE 10042587	A	14-03-2002	DE 10042587 A1 14-03-2002
		WO 0219523 A1	07-03-2002